ABSTRACT

Signal Margin Test Mode for FeRAM with Ferroelectric Reference Capacitor

The present invention provides a semiconductor memory test mode configuration. A first capacitor stores digital data and connects a cell plate line to a first bit-line through a first select transistor. The first select transistor is activated through a connection to a word line. At least one reference capacitor provides a reference voltage to a reference bit-line. A sense amplifier is connected to the first and reference bit-lines and measures a differential read signal on the first and reference bit-lines. A charge path reduces the differential read signal to determine the signal margin of the semiconductor memory.